Amendments to the Drawings:

The attached sheets of drawings include changes to FIGS. 1, 2, 3 and 7, and the addition of FIG. 1b. These sheets, which include FIGS. 1a, 1b, 2, 3 and 7, replace the original sheets including FIGS. 1, 2, 3 and 7.

In FIGS. 2, 3 and 7 lead lines have been extended to point to the proper items. In particular, the lead lines for item numbers 320a in FIG. 2, 521b in FIG. 3, and 904a in FIG. 7 have been extended.

FIG. 1b has been added to illustrate previously-omitted elements 43a and 43b, and, accordingly, FIG. 1 has been renumbered as FIG. 1a.

Attachments: Five Replacement Sheets

REMARKS

Claims 1 and 9 have been amended. No claims have been added or canceled. Accordingly, claims 1-15 remain pending in this application.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the foreign priority document.

Information Disclosure Statement

The Information Disclosure Statement filed on September 11, 2003, was identified as failing to comply with 37 CFR 1.98(a)(2). In particular, copies of pages 88-89 of *IBM TotalStorage Enterprise Storage Server Model 800,* IBM Redbooks, SG24-6424-01, Second Edition, October 2002, were alleged to have not been included with the IDS. However, a review of the Image File Wrapper for the present application on Private Pair shows that this IBM document was mistakenly scanned by the Office as the last page of one of the foreign patent documents, and in all likelihood is still present in the application file attached to the back of the foreign patent document. However, the point appears moot, since the Examiner has independently cited, considered, and applied this IBM reference, including the originally-submitted pages 88-89.

Drawings

The drawings were objected to for failing to include reference numerals 43a, 43b, and 402a mentioned in the description. In response, FIG. 1b has been added to illustrate the second embodiment of the invention described on page 13, paragraph 2. Since the second embodiment is fully described in the Specification, the addition of FIG. 1b does not constitute new matter. Reference numerals 43a and 43b and the described power units have been added to FIG. 1b. Reference numeral 402a has been deleted from the specification since this is a typographical error for referring to FIFO buffers 102b and 102a, as is clear from the next sentence of the paragraph.

The drawings were objected to in FIG. 3 as being unclear as to the item being referred to by numeral 512b. In response, the lead line for this reference number has been amended in FIG. 3.

Similarly, the drawings were objected to in FIG. 7 as being unclear as to the item being referred to by numeral 908a. In response, it is believed that the Examiner was referring to numeral 904a, as there is no numeral 908a in the application. The lead line for reference number 904a has been amended in FIG. 7.

In addition, the lead line for reference number 320a, has been similarly amended in FIG. 2 to contact the referred-to item.

Specification

The Specification has been amended to correct the misspelling of “battery” as “buttery” on page 6, line 2. Further, the Specification has been amended on page 10,

third paragraph, to define "CRC" with the commonly-understood meaning in the art. Further, the specification has been amended on pages 5, 6, 8 and 13 to add FIG. 1b and to designate original FIG. 1 as FIG. 1a. FIG. 1b illustrates the configuration described on page 13, second paragraph, of the Specification. Accordingly, the addition of FIG. 1b does not constitute new matter.

Claim Objections

Claim 1 was objected to as having a typographical error. In response, claim 1 has been amended to correct the error in the manner suggested by the Examiner.

35 USC § 103

Claims 1, 10 and 15 were rejected under 35 USC § 103(a) as being unpatentable over the IBM publication, *IBM TotalStorage Enterprise Storage Server Model 800*, (hereafter "IBM") in light of Shibata et al. (US Patent No. 5,123,099 - hereafter "Shibata"). Additionally, claims 2-7 and 11-13 were rejected under 35 USC § 103(a) as being unpatentable over IBM and Shibata, and further in view of Beardsley et al. (US Patent No. 5,437,022 - hereafter "Beardsley"). Claims 8 and 14 were rejected under 35 USC § 103(a) as being unpatentable over IBM, Shibata, and Beardsley, further in view of Yanai et al. (US Patent Application Publication No. 20030005355 - hereafter "Yanai"). Claim 9 was rejected under 35 USC § 103(a) as being unpatentable over IBM and Shibata, further in view of Matsumoto et al. (US

Patent No. 5,720,028 - hereafter "Matsumoto"). These rejections are traversed as follows.

Discussion of Invention

The present invention teaches a storage system and method of writing data in a storage system having duplex cache memory. The storage system has a plurality of control units and storage devices. Each of the control units has a first memory, which may be a cache memory, and a second memory. The second memory may be a FIFO buffer having a capacity less than that of the first memory. By this arrangement, one of the control units of the storage system that has received a request for writing data from a host system stores data corresponding to the write request in the first memory and the second memory. The host system may then be informed about a completion of the data writing. The control unit then transfers the data stored in the second memory to the first memory (i.e., the cache memory) of the other control unit. Then, since the writing from memory to disk takes considerably longer than writing from one memory to another, the data stored in the cache memories are eventually written to the disks under control of cache control algorithms, as is well known in the art.

Combination of IBM and Shibata does not Teach or Suggest the Independent Claims

Independent claims 1, 10 and 15 were rejected under the combination of IBM and Shibata, and independent claim 9 was rejected under IBM and Shibata and further in view of Matsumoto. IBM at pages 30 and 101 teaches a system in which a

nonvolatile storage (NVS) is provided in each cluster as a backup memory for a cache memory of the other cluster. In the event of cluster failure, the write data for the failed cluster will be the NVS of the surviving cluster. At pages 88 and 89 of IBM, it is described that the data is written first to the NVS, the host is notified that the write operation is complete, and a copy of the data is then transferred from the host adapter to the cache. However, when the quantity of data to be written exceeds the size of the NVS, the storage system cannot accept data subsequently sent from the host system until the data written in the cache memory is written to the disk storage devices, thereby resulting in largely deteriorated performance. Further, as set forth at page 30 of IBM, if there is a failure, the NVS is destaged to disk arrays, which takes considerably longer than the arrangement of the present invention wherein the data is stored to the second cache.

Shibata teaches a duplexed system in which, when data is written into the cache memory 3, the data is simultaneously written to a FIFO memory 4. A means is provided for writing the contents of the current FIFO memory 4 into the **standby main storage device 2'** independently of an operation of the central processing unit (see, e.g., column 4, lines 24-38, column 5, line 20, column 6, lines 10-12). Accordingly, the FIFO 4 of Shibata does not write to the duplexed cache memory 3', but to the standby main storage devices 2', which is the equivalent of writing to the disk drives 12 of the present invention. Shibata states at column 1, lines 25-39, that despite the high operation speed of the CPU, the access time for the main storage devices is long, which is why a cache is provided. Thus, since the FIFO 4 of Shibata writes to main

storage devices, rather than to a cache, Shibata suffers from the same shortcomings as the arrangement of IBM discussed above. Since the FIFO of Shibata writes directly to the main storage, the FIFO will be limited to writing at the access speed of the main storage. Further, because of the delay caused by writing to the main storage, the FIFO of Shibata may become full, thereby necessitating a cessation of writing operations (see, e.g., column 10, lines 30-37). Thus the FIFO of Shibata will be required to be quite large since it must store each write in queue as they are being written to the main storage, while the FIFO of the present invention may be considerably smaller since it must only store a write long enough to transfer it to the second cache memory. Further, because the FIFO of the present invention may be considerably smaller, any battery that powers it may also be smaller.

From the foregoing, it should be apparent that, unlike the present invention, Shibata does not provide for a true duplex of cache memories. Further, because Shibata teaches writing directly to main storage rather than to a cache, Shibata does not enable the writing of data from the cache to the main storage to be controlled by conventional algorithms, which is also unlike the present invention.

Accordingly neither Shibata, nor IBM, nor the combination thereof teach the present invention, as set forth in original claims 10 and 15, and amended claims 1 and 9, wherein the data is written to a first cache memory and a first FIFO, a response is returned to the host, and the data is then written to a second cache in a second controller, thereby providing a true duplexed cache. Under the system of the present invention the data is safely and quickly duplexed into the cache memories of both the

controllers without the risk of lost data, which is not taught by IBM or Shibata, or any combination thereof, or any of the other art of record.

The remaining claims depend from these independent claims, claim additional features of the invention, and are patentable at least because they depend from allowable base claims.

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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